What is claimed is:

1. A BISR scheme comprising:

a fuse controller;

a plurality of memories connected to the fuse controller;

a plurality of fuse blocks connected to the fuse controller, said BISR scheme configured such that said memories share said fuse blocks.

2. A BISR scheme as recited in claim 1, wherein the memories are serially connected to the fuse controller.

3. A BISR scheme as recited in claim 1, wherein the fuse blocks are serially connected to the fuse controller.

4. A BISR scheme as recited in claim 1, wherein the memories are serially connected to the fuse controller and the fuse blocks are serially connected to the fuse controller.

5. A BISR scheme as recited in claim 1, wherein there are more memories than fuse blocks.

6. A BISR scheme as recited in claim 1, wherein there fuse controller is configured to program memory addresses into the fuse blocks.

7. A BISR scheme as recited in claim 1, wherein there fuse controller is configured to program memory addresses and repair solutions into the fuse blocks.

8. A method of implementing a BISR scheme comprising:

providing a fuse controller, a plurality of memories connected to the fuse controller, and a plurality of fuse blocks connected to the fuse controller; and

having the memories share the fuse blocks.

9. A method as recited in claim 8, further comprising performing a wafer sort.

10. A method as recited in claim 8, further comprising burning the fuse blocks to program a repair solution and memory addresses.

11. A method as recited in claim 10, further comprising loading the repair solution and memory addresses into the fuse controller.

12. A method as recited in claim 8, further comprising loading fuse values into the fuse controller.